What is Claimed is:

1. A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply signal node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first plurality of feedback circuits for selectively providing a first feedback path between the second node and the first node, wherein each of said feedback circuits receives a control signal so that only one of the first plurality of feedback circuits provides the first feedback path at any one time; and

a second plurality of feedback circuits for selectively providing a feedback path between the second node and the third node, wherein each of said feedback circuits receives a control signal so that only one of the second plurality of feedback circuits provides the second feedback path at any one time.

2. The circuit of claim 1 wherein:

each feedback circuit in the first plurality of feedback circuits comprises a first feedback transistor and a second feedback transistor, the first feedback transistor having a control terminal coupled to the second node and the first feedback transistor being coupled between the power supply signal node and the second feedback transistor, the second feedback transistor having a control terminal for receiving the control signal provided to said feedback circuit and the second feedback transistor being coupled between the first feedback transistor and the first node; and

each feedback circuit in the second plurality of feedback circuits comprises a first feedback transistor and a second feedback transistor, the first feedback transistor having a control terminal coupled to the second node and the first feedback transistor being coupled between the reference node and the second feedback transistor, the second feedback transistor having a control terminal for receiving the control signal provided to said feedback circuit and the second feedback transistor being coupled between the first feedback transistor and the third node.

3. The circuit of claim 2 wherein:

the feedback transistors in each feedback circuit in the first plurality of feedback circuits have a combined conductivity that is different from the combined conductivity of the feedback transistors in any other feedback circuit in the first plurality of feedback circuits; and

the feedback transistors in each feedback circuit in the second plurality of feedback circuits have a combined conductivity that is different from the combined conductivity of the feedback transistors in any other feedback circuit in the second plurality of feedback circuits.

4. The circuit of claim 2 wherein:

the first transistor, the second transistor, and the feedback transistors in each feedback circuit in the first plurality of feedback circuits are of a first type; and

the third transistor, the fourth transistor, and the feedback transistors in each feedback circuit in the second plurality of feedback circuits are of a second type.

5. The circuit of claim 4 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

6. The circuit of claim 5 wherein:

the first feedback transistor in each feedback circuit in the first plurality of feedback circuits has a different threshold voltage magnitude from that of the first feedback transistor in any other feedback circuit in the first plurality of feedback circuits; and

the first feedback transistor in each feedback circuit in the second plurality of feedback circuits has a different threshold voltage magnitude from that of the first feedback transistor in any other feedback circuit in the second plurality of feedback circuits.

7. The circuit of claim 4 wherein

a source terminal of the first transistor is coupled to the reference node and a drain terminal of the first transistor is coupled to the first node;

a source terminal of the second transistor is coupled to the first node and a drain terminal of the second transistor is coupled to the second node;

a drain terminal of the third transistor is coupled to the second node and a source terminal of the third transistor is coupled to the third node;

a drain terminal of the fourth transistor is coupled to the third node and a source terminal of the fourth transistor is coupled to the power supply signal node;

in each feedback circuit in the first plurality of feedback circuits, a drain terminal of the first feedback transistor is coupled to the power supply signal node, a source terminal of the first feedback transistor is coupled to a drain terminal of the second feedback transistor, and a source terminal of the second feedback transistor is coupled to the first node; and

in each feedback circuit in the second plurality of feedback circuits, a drain terminal of the first feedback transistor is coupled to the reference node, a source terminal of the first feedback transistor is coupled to a drain terminal of the second feedback transistor, and a source terminal of the second feedback transistor is coupled to the third node.

8. The circuit of claim 1 wherein the first and second plurality of feedback circuits each consists of first and second feedback circuits, wherein the first feedback circuits in each plurality of feedback circuits receive a common control signal and the second feedback circuits in each plurality of feedback circuits receive a complementary version of said common control signal.

9. The circuit of claim 1 wherein the control signals provided to each feedback circuit are programmable settings.

10. A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled

between the second node and a third node, and a fourth transistor coupled between the third node and a power supply signal node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a plurality of first feedback circuits for selectively providing a first feedback path between the second node and the first node, wherein each of the first feedback circuits receives a control signal so that only one of the first feedback circuits provides the first feedback path at any one time; and

a second feedback circuit for providing a second feedback path between the second node and the third node.

11. The circuit of claim 10 wherein:

each first feedback circuit comprises a first feedback transistor and a second feedback transistor, the first feedback transistor having a control terminal coupled to the second node and the first feedback transistor being coupled between the power supply signal node and the second feedback transistor, the second feedback transistor having a control terminal for receiving the control signal provided to said feedback circuit and the second feedback transistor being coupled between the first feedback transistor and the first node; and

the second feedback circuit comprises a feedback transistor having a control terminal coupled to the second node and said feedback transistor being coupled between the reference node and the third node.

12. The circuit of claim 11 wherein:

the feedback transistors in each of the plurality of first feedback circuits have a combined conductivity that is different from the combined conductivity of the feedback transistors in any other first feedback circuit.

13. The circuit of claim 11 wherein:

the first transistor, the second transistor, and the feedback transistors in each of the plurality of first feedback circuits are of a first type; and

the third transistor, the fourth transistor, and the feedback transistor in the second feedback circuit are of a second type.

14. The circuit of claim 13 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

15. A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply signal node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first feedback circuit for providing a first feedback path between the second node and the first node; and

a plurality of second feedback circuits for selectively providing a second feedback path between the second node and the third node, wherein each of the second feedback circuits receives a control signal so that only one of the second feedback circuits provides the second feedback path at any one time.

16. The circuit of claim 15 wherein:

the first feedback circuit comprises a feedback transistor having a control terminal coupled to the second node and the feedback transistor being coupled between the power supply signal node and the first node; and

each feedback circuit in the plurality of second feedback circuits comprises a first feedback transistor and a second feedback transistor, the first feedback transistor having a control terminal coupled to the second node and the first feedback transistor being coupled between the reference node and the second feedback transistor, the second feedback transistor having a control terminal for receiving the control signal provided to said feedback circuit and the second feedback transistor being coupled between the first feedback transistor and the third node.

17. The circuit of claim 16 wherein:

the feedback transistors in each of the plurality of second feedback circuits have a combined conductivity that is different from the combined conductivity of the feedback transistors in any other second feedback circuit.

18. The circuit of claim 16 wherein:

the first transistor, the second transistor, and the feedback transistor in the first feedback circuit are of a first type; and

the third transistor, the fourth transistor, and the feedback transistors in each of the plurality of second feedback circuits are of a second type.

19. The circuit of claim 18 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

20. A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a first plurality of independent feedback circuits, each providing a different effect on the upper trip point level when selected, and a second plurality of independent feedback circuits, each providing a different effect on the lower trip point level when selected, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one feedback circuit in the first plurality of feedback circuits and one feedback circuit in the second plurality of feedback circuits.

21. The circuit of claim 20 wherein the feedback circuits in the first plurality of feedback circuits comprise n-channel metal oxide semiconductor field-effect transistors, and the feedback circuits in the second plurality of feedback circuits comprise p-channel metal oxide semiconductor field-effect transistors.

22. The circuit of claim 21 wherein:

the transistors in each feedback circuit in the first plurality of feedback circuits have a combined conductivity that is different from the combined conductivity of the

feedback transistors in any other feedback circuit in the first plurality of feedback circuits; and

the transistors in each feedback circuit in the second plurality of feedback circuits have a combined conductivity that is different from the combined conductivity of the feedback transistors in any other feedback circuit in the second plurality of feedback circuits.

23. The circuit of claim 20 wherein the one or more control signals are programmable settings.

24. A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a plurality of independent feedback circuits each providing, when selected, a different effect on one of the upper trip point level and the lower trip point level, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one feedback circuit in the plurality of feedback circuits.

25. A method of providing an adjustable hysteresis characteristic in a Schmitt trigger circuit comprising:

providing one or more control signals to the Schmitt trigger circuit; and

in response to the one or more control signals, selecting one of a first plurality of independent feedback circuits to provide a first desired feedback path in the Schmitt trigger circuit.

26. The method of claim 25 further comprising:

in response to the one or more control signals, selecting one of a second plurality of independent feedback circuits to provide a second desired feedback path in the Schmitt trigger circuit.

27. The method of claim 25 comprising providing the one or more control signals based on the voltage level of a power supply signal in the Schmitt trigger circuit.

28. The method of claim 25 comprising programmably providing the one or more control signals .